

**REMARKS**

Claims 1-18 are pending in the application, with claims 1, 7 and 13 being the independent claims. Based on the following Remarks, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections.

***Rejections under 35 U.S.C. § 102(e)***

Claims 1-18 are rejected under 35 U.S.C. § 102(e) as being allegedly unpatentable over U.S. Patent No. 6,336,158 (hereinafter referred to as “the Martwick patent”). Applicant respectfully traverses these rejections since the Martwick patent does not teach each element of independent claims 1, 7 and 13 for at least the following reason.

Independent claims 1, 7 and 13 each includes the similar feature of a decoder to provide bus segment information to the bridge independently of response to a bus transaction on the second data bus initiated by a source device. Independent claims 1, 7 and 13 were amended in response to the first non-final office action to include what the Applicant referred to as the “connection feature.” The connection feature defines how the decoder is able to provide bus segment information to the bridge independently of response to a bus transaction on the second data bus initiated by a source device. In the present invention, via the connection feature, it is the associated bus segment of the asserted connection that the decoder uses to generate the bus segment information.

Applicant respectfully disagrees with the Examiner that the Martwick patent teaches the connection feature of independent claims 1, 7 and 13. The Examiner states that the

connection feature is taught by connection bus 103 coupled to source device 110 is associated with bus segment 102 coupled to target device 112, when decoder (I/O controller) 108 enables bi-directional communication between said devices. The Martwick patent discloses that, upon receipt of an address, the I/O controller 108 checks to see whether information corresponding to the received transaction address is already contained in the I/O map cache. If no match is found in the I/O map cache, the I/O controller 108 then proceeds to snoop the I/O decode map with the present transaction address to retrieve relevant decode information (see, e.g., col 7, lines 15-23 of the Martwick patent). Thus, it is through the use of the I/O map cache and I/O decode map that the I/O controller 108 of the Martwick patent retrieves relevant decode information and not via the connection feature of the claimed invention. Accordingly, the Martwick patent does not teach the connection feature of independent claims 1, 7 and 13. Therefore, for at least this reason, independent claims 1, 7 and 13 (and their dependent claims 2-6, 8-12 and 14-18) are patentable over the Martwick patent under 35 U.S.C. § 102(e). Accordingly, Applicant requests that the rejections under 35 U.S.C. § 102(e) be reconsidered and withdrawn.

Appln. Serial No. 10/028,881  
Reply to Final Office Action mailed on January 19, 2005

**INVITATION FOR A TELEPHONE INTERVIEW**

The Examiner is invited to call the undersigned, Molly A. McCall, at (703) 633-3311  
if there remains any issue with allowance of the case.

**CONCLUSION**

Applicant respectfully submits that all of the stated grounds of rejection have been properly traversed accommodated or rendered moot. Applicant believes that a full and complete response has been made to the outstanding Office Action. Thus, Applicant believes that the present application is in condition for allowance, and as such, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections, and allowance of this application.

Respectfully submitted,

Intel Corporation

Dated: 3-17-05

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3-17-05  
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